IN THE CLAIMS:

Claim 1. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal ~~generator~~ generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals.

Claim 2. (Original) A semiconductor integrated circuit according to claim 1, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals; and

a composite circuit for synthesizing the pulses to generate said main power-on reset signal.

Claim 3. (Canceled)

Claim 4. (Currently amended) A semiconductor integrated circuit ~~according to claim 3~~ comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal,

wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 5. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal ~~generator~~ generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals and said external power-on reset signal.

Claim 6. (Original) A semiconductor integrated circuit according to claim 5, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 7. (Currently amended) A method of initializing a semiconductor integrated circuit comprising the steps of:

generating a plurality of pulse signals as power-on reset signals according to a plurality of sub power-on reset signals at timings different from each other, and independently of each other, at least one of said pulse signals including a rectangular pulse; and

initializing an internal circuit according to at least one from any of said power-on reset signals.

Claim 8. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal ~~generator~~ generators, including transistors having threshold values, for generating a plurality of sub power-on reset signals on basis of the respective threshold values of each of the transistors, and independently of each other; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signals.

Claim 9. (Currently amended) A semiconductor integrated circuit comprising:

a first sub reset signal generator, including a first transistor having a first threshold ~~voltage~~ value, for generating a first sub power-on reset signal on basis of the first threshold ~~voltage~~ value;

a second sub reset signal generator, including a second transistor having a second threshold value, for generating a second sub power-on reset signal on basis of

the second threshold ~~voltage~~ value, independently of the first sub reset signal generator; and

a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one of the first sub power-on reset signal and the second sub power-on reset signal.

Claim 10. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal ~~generator~~ generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other;

a plurality of pulse generators for generating pulses on the basis of the plurality of sub power-on reset signals, respectively, at least one of said pulses being a rectangular pulse; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

Claim 11. (Currently amended) A method of initializing a semiconductor integrated circuit having a plurality of sub reset signal ~~generator~~ generators including transistors having threshold values, the method comprising the steps of:

generating a plurality of sub power-on reset signals, according to respective threshold values of each of the transistors, and independently of each other;

generating a plurality of pulse signals as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other, at least one of said pulse signals including a rectangular pulse; and

initializing an internal circuit according to at least one of said power-on reset signals.

Claim 12. (Original) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals, wherein said main reset signal generator includes:

a plurality of pulse generators for respectively generating pulses which are shorter than an interval between transition edges of said sub power-on reset signals; and

a composite circuit for synthesizing the pulses to generate said main power-on reset signal.

Claim 13. (Canceled)

Claim 14. (Currently amended) A semiconductor integrated circuit ~~according to claim 13~~ comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal supplied from the exterior of the semiconductor integrated circuit; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal,

wherein said main reset signal generator comprises:

a plurality of pulse, wherein each pulse generator generates a respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal;, and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 15. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal ~~generator~~ generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other;

a reset terminal for receiving an external power-on reset signal supplied from the exterior of the semiconductor integrated circuit; and

a main reset signal generator for generating a rectangular pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals and said external power-on reset signal.

Claim 16. (Original) A semiconductor integrated circuit according to claim 15, wherein said main reset signal generator comprises:

a plurality of pulse generators, wherein each pulse generator generates a respective pulse on the basis of a respective transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Claim 17. (Original) A method of initializing a semiconductor integrated circuit comprising the steps of:

generating a plurality of power-on reset signals as pulse signals according to a plurality of sub power-on reset signals at timings different from each other, the pulse signals being shorter than an interval between transition edges of said sub power-on reset signals; and

initializing an internal circuit according to at least one from any of said power-on reset signals.

Claim 18. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of sub reset signal ~~generator~~ generators for generating a plurality of sub power-on reset signals at timings different from each other, and independently of each other; and

a main reset signal generator for generating a main power-on reset signal to initialize an internal circuit, according to at least one of said plurality of sub power-on reset signals, wherein

said main reset signal generator generates said main power-on reset signal having pulses respectively corresponding to each of said sub power-on reset signals, when threshold values of transistors formed in said semiconductor integrated circuit are typical values.

Claim 19. (Canceled)

Claim 20. (Currently amended) A method of initializing a semiconductor integrated circuit having a plurality of sub reset signal ~~generator~~ generators including transistors having threshold values, the method comprising the steps of:

generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors, and independently of each other;

generating a plurality of pulse signals as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other, said power-on reset signals having pulses not overlapping each other when threshold values of transistors formed in said semiconductor integrated circuit are typical values; and

initializing an internal circuit according to at least one of the pulses of said power-on reset signals.